United States Patent [19]

Hedde

[11] **3,810,160**

[45] **May 7, 1974**

[54] **SWITCHING MATRIX**

[76] Inventor: **Jean Hedde,** 1, rue des Platenes, 91 Orsay, France

[22] Filed: **Nov. 9, 1972**

[21] Appl. No.: **305,061**

[30] **Foreign Application Priority Data**

Nov. 16, 1971 France 71.40895

[52] **U.S. Cl.** ..... **340/166 R**

[51] **Int. Cl.** **H04q 3/00**

[58] **Field of Search** ..... 340/166 R

[56] **References Cited**

UNITED STATES PATENTS

3,609,546 9/1971 Magnusson ..... 340/166 X

Primary Examiner—Harold I. Pitts

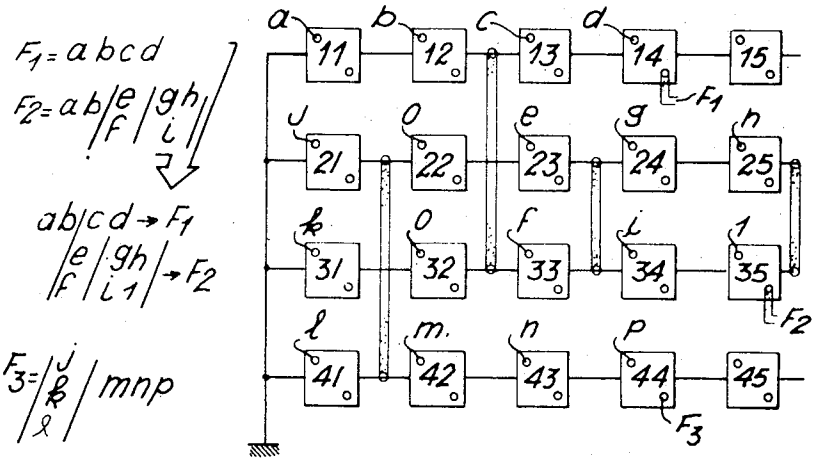
Attorney, Agent, or Firm—Lane, Aitken, Dunner & Ziems

[57] **ABSTRACT**

A switching matrix for realizing at least one or more transcoding function having a constant switching time-delay between different binary variables comprises an array of identical switching circuits disposed in the form of a matrix table having *n* lines and *m* columns. Each circuit comprises an input terminal C, an input terminal E of said applied binary variable, an output terminal L and an auxiliary output terminal S which supplies the complemented value of the value which appears at the output terminal L. Each succeeding circuit on a line has an input C coupled to the output L of the preceeding circuit which is located on the same line and each preceeding circuit on a line has an output L coupled to the input C of the following circuit which is located on the same line. The inputs C of the circuits of the first column are all connected to ground. Means for provide selected connections between different circuits through the intermediary of the terminals L, E and S and means are provided for applying said binary variables to said terminals E. The structure of each circuit is such as to have the following relations between the input and output values :

$$S = E \cdot \text{AND} \cdot C \text{ and } \bar{L} = \bar{S}.$$

2 Claims, 7 Drawing Figures



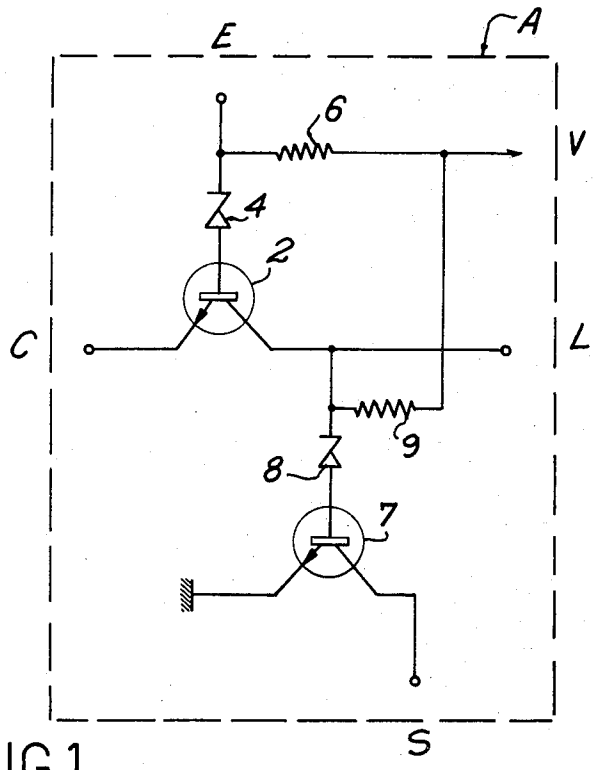


FIG.1

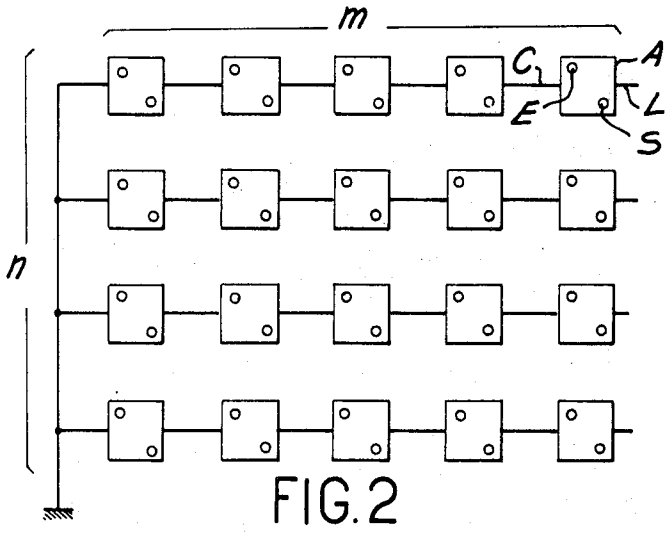


FIG.2

$F_1 = a\,b\,c\,d$

$F_2 = a\,b \,/\, \begin{matrix} e \\ f \end{matrix} \,/\, \begin{matrix} g\,h \\ i \end{matrix}$

$ab \,/\, cd \rightarrow F_1$

$\begin{matrix} e \\ f \end{matrix} \,/\, \begin{matrix} g\,h \\ i\,1 \end{matrix} \rightarrow F_2$

$F_3 = \begin{matrix} j \\ k \\ l \end{matrix} \,/\, m\,n\,p$

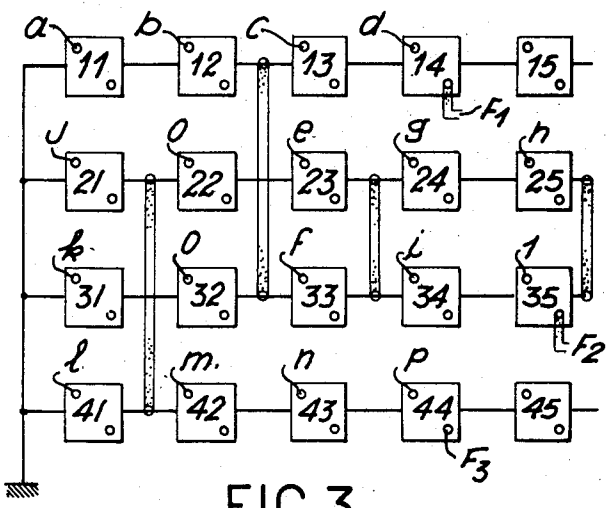


FIG. 3

$F(ab) = \begin{matrix} a \\ b \end{matrix} \,/\, \begin{matrix} \bar{b} \\ \bar{a} \end{matrix} = \begin{matrix} a\,\bar{b} \\ b\,\bar{a} \end{matrix}$

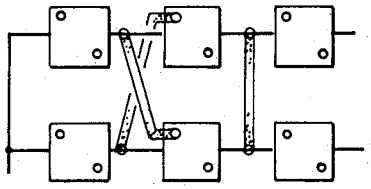


FIG. 4

$F(abcd) = F(ab).\bar{F}(cd) \,/\, F(cd).\bar{F}(ab)$

$= \begin{matrix} a\,\bar{b} \\ b\,\bar{a} \\ c\,\bar{d} \\ d\,\bar{c} \end{matrix} \,/\, \begin{matrix} c\,\bar{d} \\ \bar{d}\,\bar{c} \\ a\,\bar{b} \\ \bar{b}\,\bar{c} \end{matrix}$

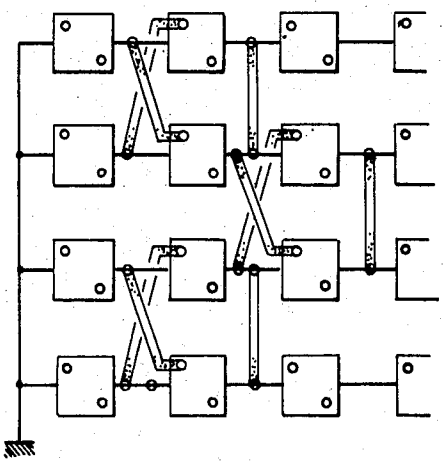
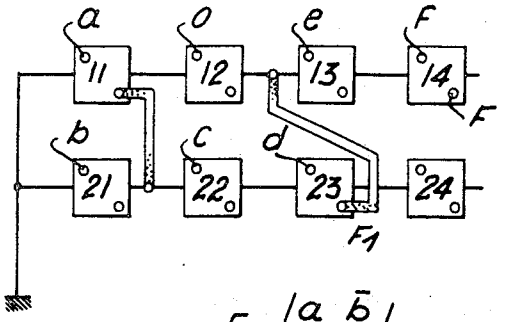


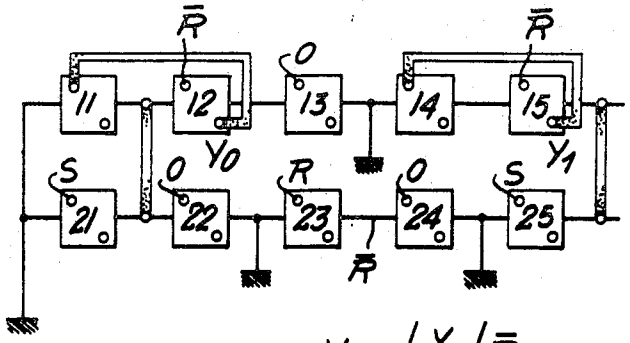
FIG. 5

FIG.6



$$F = \left/ \begin{matrix} a & \bar{b} \\ \bar{c} & \\ \bar{d} & \end{matrix} \right/ ef$$

FIG.7



$$Y_0 = \left/ \begin{matrix} Y_0 \\ S \end{matrix} \right/ \bar{R}$$

$$Y_1 = \left/ \begin{matrix} Y_1 & \bar{R} \\ S & \end{matrix} \right/$$

SWITCHING MATRIX

BACKGROUND OF THE INVENTION

This invention relates to a switching matrix which is formed from switching circuits having two states depending on the values (logical level 0 or 1) which are applied to the two inputs of said circuits. A switching matrix is a device in which the components are each equivalent to a switch and disposed in the form of a matrix; this device serves to realize a transcoding function, that is to say to produce at the output binary values which are dependent on input binary variables applied in each case at one of the inputs of the matrix. This matrix can advantageously be employed for the automation of industrial processes such as the control and regulation of physical quantities (temperature, pressure, flow rate and the like), opening and closure of valves, switching-on of apparatus, and so forth.

The binary switching matrices of the prior art make use of Boolean algebra. These devices are logic circuits formed from elementary circuits which arise from the application of Boolean algebra (for example AND and OR circuits) and a single device which usually serves to realize a single transcoding function. The different elements are connected to a printed circuit which is specially designed for the realization of said transcoding function. The realization of another function by means of this apparatus entails the need to modify the printed circuit and it is more advantageous in that case to provide a new device. Similarly, the replacement of one elementary circuit by another calls for a further study of the connections between elements and complete rewiring is therefore necessary. Moreover, Boolean algebra is written in a linear manner and the study of the location of the different elementary circuits in order to form a logic circuit does not readily lend itself to this type of linear writing. When the number of input binary variables is large, the simplifications which can be made in the realization of logical functions are not evident.

SUMMARY OF THE INVENTION

The present invention proposes a switching matrix and a switching circuit which corresponds to practical requirements more effectively than those of the prior art, especially insofar as the matrix permits a simpler design of the logic circuits, ready modification of these circuits and the use of a single elementary circuit, this being achieved by employing a formalism of writing of a binary analysis which is different from Boolean algebra.

To this end, the invention proposes a switching matrix for realizing at least one transcoding function having a constant switching time-delay between different binary variables, characterized in that it comprises an array of switching circuits which are all identical and disposed in a matrix table having n lines and m columns, each circuit comprising an input terminal C proper of said circuit and an input terminal E of said applied binary variable, an output terminal L proper of said circuit and an auxiliary output terminal S which supplies the complemented value of the value which appears at said output terminal L proper, a circuit having an input C proper coupled to the output L proper of the aforesaid circuit which is located on the same line and an output L proper coupled to the input C proper of the following circuit which is located on the same line, the inputs C proper of the circuits of the first column being all connected to ground, means for providing connections between different circuits through the intermediary of the terminals L, E and S and means for applying said binary variables to said terminals E, the structure of each circuit being such as to have the following relations between the input and output values :

$$S = E \cdot \text{AND} \cdot \overline{C} \text{ and } L = \overline{S}$$

In accordance with a further characteristic feature, the matrix is characterized in that each circuit is constituted by a first transistor in which the base is coupled to the input E of the binary variable through a Zener diode, an emitter which is coupled solely to the input C proper and a collector which is coupled to the output L proper, by a first biasing resistor connected between said binary variable input E and a bias voltage source, a second transistor having a grounded emitter, a collector which is coupled to the auxiliary output S and a base which is connected through a Zener diode to the collector of said first transistor, and by a second biasing resistor connected between said voltage source and the collector of said first transistor.

This invention will be more readily understood from a perusal of the following description in which embodiments of the invention are given by way of explanatory example but without implying any limitation, reference being made to the accompanying drawings, wherein :

DESCRIPTION OF THE DRAWINGS

FIG. 1 is an electrical diagram of said switching circuit;

FIG. 2 shows diagrammatically one form of construction of the switching matrix;

FIGS. 3 to 7 show by way of example the realization of different transcoding functions by means of said matrix.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The switching matrix is not based on the application of Boolean algebra but on a novel formalism of a binary analysis as devised by Andre Blanchard and described in the book entitled "Elements de commutation generale et leurs applications aux systemes de telephonie automatique" (General switching elements and their applications to automatic telephone systems) (published by Eyrolles, 1962). This formalism has been developed by R.L. Vallee in the book entitled "Analyse binaire" (published by Masson, 1970). If we make use of n binary functions $a, b, c, \ldots$ each of which can assume the algebraic value 0 or 1, the principal characteristics of this binary analysis are as follows :

the algebraic product P of these functions is also a binary function :

$$P = a \cdot b \cdot c \cdot \ldots$$

The product P which is usually known as the "AND" function at the time of its applications is equal to unity when all the functions in factor are simultaneously equal to unity and zero if only one of these functions is zero ;

the complementary state of the binary functions a, b, c, . . . which should be written $\bar{a}$, $\bar{b}$, $\bar{c}$ ... is obtained by means of the following algebraic expressions :

$$\bar{a} = 1 - a$$
$$\bar{b} = 1 - b$$
$$\bar{c} = 1 - c$$

The term "duality" designates the relation which exists between a function and its complement, that is to say :

$$a + \bar{a} - 1 = 0$$

from this duality relation and from the product, it is possible to define another function which, with respect to the value 0 (and the value 1), plays a part which is symmetrical with the part played by the product with respect to the value 1 (and the value 0). This new function π can be written :

$$\pi = \bar{a} \cdot \bar{b} \cdot \bar{c} \cdot \ldots$$

namely algebraically :

$$\pi = 1 - [\,(1-a)\,(1-b)\,(1-c)\ldots\,]$$

This function, which is designated by the author of this binary analysis as "Produel" and usually known as the "OR" function at the time of its applications is zero when all all its terms a, b, c, . . . are simultaneously zero and equal to unity if only one of these terms is equal to unity. It is said that the terms a, b, c, . . . are in dual factor. It is proposed to represent the "Produel" π function by grouping together the terms which compose this latter in a vertical column by analogy with the horizontal writing of the product P and in order to represent in this new symbolism the property of duality :

$$\pi = \left|\begin{matrix} a \\ b \\ \\ c \\ \cdot \\ \cdot \end{matrix}\right|$$

the main properties which are common to the product P and to the produel π are commutativity, associativity, idempotence (or in other words $a^n = a$) and reciprocal distributivity.

Thus, the function (a AND b) OR (c AND d) is written :

$$\left|\begin{matrix} a & b \\ c & d \end{matrix}\right|$$

and the function (a OR c) AND (b OR d) is written :

$$\left|\begin{matrix} a & b \\ c & d \end{matrix}\right|$$

Whereas in accordance with the Boolean algebra the transcoding functions are written linearly, they are written by means of this formalism in accordance with a generally two-dimensional matrix, in which the "AND" functions correspond to horizontal reading of this matrix and the "OR" functions correspond to vertical reading. The application of this writing formalism to the formation of a transcoding matrix complies both vertically and horizontally with this form of writing, which is not possible with the Boolean algebra. The immediate advantage for the realization of logical functions is apparent since it is only necessary to interconnect the elementary switching circuits by following exactly the result of the binary analysis.

Instead of the letters a, b, c, . . . , one imagines a series of switches connected in series and/or in parallel and supplied from a current source. The main difficulty consisted in changing-over from a switch to a single elementary switching circuit which makes use of transistors. The construction of the transcoding matrix in accordance with the present invention is carried out by means of a single switching circuit. This latter is shown diagrammatically in FIG. **1.**

The switching circuit A in accordance with the present invention has four terminals: an input terminal C proper of the circuit, an output terminal L proper of the circuit, an input terminal E of the binary variable in the switching circuit and finally an auxiliary output terminal S having values which are interrelated by the expressions : $S = E \cdot \bar{C}$ $L = \bar{S}$. The circuit A comprises a first transistor **2,** the base of which is coupled to the input E through a Zener diode **4.** The emitter of said transistor is coupled directly and solely to the input C and its collector is connector to the output terminal L without any load resistance connected to the potential V, the resistor **9** being solely intended to apply a bias voltage to the base of a second transistor **7.** A bias resistor **6** is connected between the input E of the binary variable and the source of bias voltage V. The base of the second transistor **7** is connected to the collector of the transistor **2** through a Zener diode **8.** The collector of the transistor **7** is connected directly to the auxiliary output S and the emitter of said transistor is connected to ground. A bias resistor **9** is connected between said voltage source V and the collector of the transistor **2.** Each base of the two transistors **2** and **7** can be connected to ground through a bias resistor which is not shown in the drawings, but this resistor is not essential. The transistor **2** operates in the same manner as a contact having a non-zero residual resistance which is compensated by the Zener diode **4.** The Zener voltage of the diode **8** must be considerably higher than the collector-emitter saturation voltage of the transistor **2.** The transistor **7** complements and regenerates the signal which is applied to its base. This transistor can be chosen so as to permit, if necessary, the passage of a saturation current of sufficiently high value to drive directly an external element of medium power. When the input C of the circuit is connected to ground (logical level 0), the logical values of the output L and of the output S can assume two different states according to the value of the binary variable which is applied to the input E. The circuit A therefore has two different states.

The switching circuit can advantageously be employed for the construction of a switching matrix which utilizes the formalism of the binary analysis as explained in the foregoing. This matrix is shown diagrammatically in FIG. **2.** It comprises an array of elementary circuits A as shown in FIG. **1,** these circuits being arranged in the form of a matrix table having m lines and n columns. The connections between the emitters of the transistors **7** and ground as well as the connections between the resistors **6** and **9** and the source of bias voltage V are not shown. The circuits A of any one line are connected in series; in other words, the input terminal C of each circuit A is connected to the terminal L of the preceding circuit and the terminal L of the circuit considered is connected to the input terminal C of

the following circuit. The inputs C of all the circuits A of the first column are connected to ground. The Zener voltage of each diode **4** and **8** must be higher than the sum of the collector-emitter saturation voltages of the series-connected transistors **2**. By way of example, if there is connected between the input E of an elementary circuit and ground a resistor which is varied from 0 ohms, the transistor **2** of said circuit remains in the cut-off or non-conducting state as long as the voltage of its base is lower than the Zener voltage of the diode **4**, namely as long as said resistance remains lower than a fairly substantial predetermined value (a few kilohms): this resistance corresponds to the sum of residual resistances of a large number of series-connected transistors **2** in the saturated state.

In order that the mode of operation of the transcoding matrix may be more readily understood, each circuit A can be compared with an open or closed contact and each line of the matrix can be considered as a series of unidirectional contacts each controlled by its input E. Two series-connected elementary circuits A with the input C of the first circuit being connected to ground, deliver at the output S of the second circuit the logical AND function between the binary variables which are each applied to the two inputs E of the two circuits in series. The matrix comprises means for establishing vertical and oblique connections corresponding to connections of the elementary circuits in parallel. Said vertical and oblique connections can be established between the terminals L, E and S of the different circuits. Thus, if two switching circuits A are placed in parallel with their terminals C connected to ground and their output terminals L connected to each other, said two circuits in parallel will deliver at their output S the logical OR function between the two binary variables which are applied to their two inputs E. Any one line of the matrix can be employed partially for functions which are independent of each other: to this end, it is only necessary to place between the two parts employed an elementary circuit A whose input E is placed at the logical level 0. The mode of operation and utilization of the switching matrix as well as the utility of the terminals of the auxiliary outputs S will become more readily apparent from a perusal of the following examples of realization of transcoding functions.

Any logical function which is realized in this matrix by means of vertical connections between terminals L to the exclusion of the oblique connections between terminals S and L or between terminals L and E has a very short and constant switching time-interval irrespective of the complexity of the function. It is practically impossible to achieve this constancy of switching interval by means of conventional circuits.

The switching matrix which is illustrated in FIG. **3** comprises by way of example four lines and five columns, the elementary switching circuits A being designated by the references **11** to **45**. It is desired to realize by means of this matrix the transcoding functions

$$F_1 = abcd \text{ and } F_2 = ab \begin{vmatrix} e \\ f \end{vmatrix} \begin{vmatrix} gh \\ i \end{vmatrix} \text{ and } F_3 = \begin{vmatrix} j \\ k \\ l \end{vmatrix} mnp$$

in which the two first functions F_1 and F_2 have "*ab*" as a common portion. In FIG. **3**, the simplified and condensed writing of the two functions F_1 and F_2 is indicated. By means of a single wiring connection F_1 and F_2 will therefore be obtained simultaneously. The two circuits **11** and **12** realize the AND function between the two binary variables *a* and *b*. The function ab is therefore obtained at the output L of the circuit **12**. The realization of the function $F_1 = abcd$ is obtained simply by applying the binary variables *a*, *b*, *c*, and *d* to the input terminals E of the circuits respectively **11, 12, 13** and **14**, the series connection of the four circuits **11, 12, 13** and **14** being already performed since all the elementary circuits of any one line of the matrix are connected in series. The transcoding function F_1 is obtained at the output S of the circuit **14**. The logical OR function between the two binary variables *e* and *f* is obtained by placing the outputs L of the two circuits **23** and **33** in parallel, the binary variables *e* and *f* being applied to the input terminals E of said circuits. The logical AND operation between the two binary variables *g* and *h* is carried out by the circuits **24** and **25** which are placed in series; the same applies to the "*i* l" operation performed by the circuits **34** and **35**. A circuit whose input E is at the logical level **1** (and isolated from ground) serves as a connection from the left-hand side towards the right-hand side between two circuits (circuit **35** in FIG. **3**). The logical OR operation between *g*, *h*, and *i* is obtained by connecting the outputs L of the two circuits **25** and **35** in parallel. The transcoding function F_2 is thus obtained at the terminal S of the switching circuit **35**. In order to isolate the two elementary circuits **23** and **33** from the circuits **21** and **31**, the input E of the two circuits **22** and **32** is placed at the logical level O (by connecting to ground).

The transcoding function F_3 is obtained in accordance with the same wiring process by connecting in parallel the outputs L of the circuits **21, 31** and **41** to which are applied respectively the binary variables *i*, *k*, *l*, and also by applying the binary variables *m*, *n* and *p* to the inputs E of the circuits **42, 43** and **44** respectively, the three circuits just mentioned being pre-wired in series. The function F_3 is obtained at the output S of the elementary circuit **44**. By means of a single transcoding matrix, there have thus been obtained three functions F_1, F_2 and F_3, the first two functions having a common portion and the third function F_3 being totally independent from the two others. This number of transcoding functions which it is possible to obtain by means of a single matrix is not limitative: it depends solely on the number of elementary circuits which make up the matrix and on the complexity of the transcoding functions to be written.

FIG. **4** shows the realization of the "exclusive-OR" function having two variables *a* and *b*. The achievement of this function F (*a*, *b*,) entails the need to obtain the variables $\bar{a}$ and $\bar{b}$; these latter designate the complemented values of the variables *a* and *b*. It is worthy of note that the complemented values are obtained directly at the outputs L of the elementary circuits. Thus in FIG. **4**, in complemented variable $\bar{a}$ is obtained at the output L of the elementary circuit **11** which receives the variable *a* at its input E and the value $\bar{b}$ is obtained at the output L of the elementary circuit **21** which receives the variable *b*. The inputs E of the circuits **12** and **22** therefore receive the complemented variables $\bar{a}$ and $\bar{b}$. The function F (*a*, *b*) is realized by connecting the outputs L of the circuits **12** and **22** in parallel, the

function F (a, b) being obtained at the output S of the circuit **22** or **12.**

FIG. **5** shows the realization of the transcoding function F ($abcd$), namely the "exclusive-OR" function with four variables. This function is a generalization of the preceding function F (ab). The writing of this function having four variables by means of the formalism of the binary analysis is shown in FIG. **5.** In this figure, attention is drawn to the manner in which the complemented variables are obtained. The function F (a,b,c,d,) is obtained at the terminal S of the elementary circuit **33** or **23.**

FIGS. **4** and **5** clearly show the manner in which the complemented variables are obtained from direct variables by means of connections $L_i \longrightarrow E_j$ between the terminals L and E of two circuits i and j. As a general rule, any terminal L_i which is connected to an input E_j transmits to this latter the binary value $\bar{S}_i$, this being the complemented value of the binary value which appears at the output S_i whereas, in the case of any other connection $L_i \longrightarrow L_j$, no complementation need be taken into consideration. Similarly, a connection between an output S_i and an output L_j is equivalent to a vertical connection between L_j and L_i after complementation of the value S_i of the elementary circuit i. This last-mentioned characteristic is brought out by means of the example given in FIG. **6.**

In this example, it is desired to realize the function

$$F = \left| \begin{matrix} a & \bar{b} \\ \bar{c} & \\ \bar{d} & \end{matrix} \right| ef.$$

In this function, the number of complemented variables can be reduced by partial complementation of the function F. Thus, by setting

$$F_1 = \left| \begin{matrix} a & \bar{b} \\ \bar{c} & \\ \bar{d} & \end{matrix} \right|$$

the complemented function $\overline{F_1}$ of the function F_1 is written :

$$\overline{F_1} = \left| \begin{matrix} \bar{a} \\ b \end{matrix} \right| cd$$

At the terminals S of the circuits **21, 22, 23, 13** and **14,** we obtain :

$$S_{21} = \left| \begin{matrix} \bar{a} \\ b \end{matrix} \right| \qquad S_{22} = \left| \begin{matrix} \bar{a} \\ b \end{matrix} \right| c$$

$$S_{23} = \left| \begin{matrix} \bar{a} \\ b \end{matrix} \right| cd = \overline{F_1} \qquad S_{13} = \left| \begin{matrix} 0 \\ F_1 \end{matrix} \right| e = F_1 e$$

and

$$S_{14} = F_1 ef = F$$

It should be noted that the circuits **11** and **13** are isolated by representing the logical state O on the input terminal E of the elementary circuit **12.**

The examples of realization of transcoding functions which are given in FIGS. **3, 4, 5** and **6** demonstrate three types of connections : $L \longrightarrow L$, $L \longrightarrow E$, and $S \longrightarrow L$, thereby endowing the transcoding matrix with high flexibility of operation. It is worthy of note that the type of connection $S \longrightarrow L$ is not essential for the purpose of realizing transcoding functions, these connections being simply very practical insofar as they permit a reduction in the number of connections necessary and increase the performance potentialities of the matrix but at the expense of the total switching time. The connections $L \longrightarrow E$ ensure the complementation of the variables, the connections $L \longrightarrow L$ (parallel connection of circuits) serve to write OR functions and the series connections $L \longrightarrow C$ which are pre-wired in the matrix in the case of any one line serve to write the AND function; the two last-mentioned types of connections are an accurate reproduction of the symbolism of writing of the binary analysis already mentioned and ensure a total switching time which is independent of the function to be realized.

FIG. **7** shows by way of example the realization of the transcoding functions of

$$y_0 = \left| \begin{matrix} y_0 \\ S \end{matrix} \right| \bar{R}$$

wherein R has priority
and

$$y_1 = \left| \begin{matrix} y_1 \\ S \end{matrix} \right| \bar{R}$$

wherein S has priority

These functions are known as "memory functions." The realization of these memory functions by means of the matrix in accordance with the invention shows that this latter permits the realization of so-called "reflex" functions and the construction of sequential systems.

The elementary circuits A can be constructed in different ways: by means of discrete elements, printed circuits or integrated circuits. For example, it is possible to construct a module in an integrated circuit in which a plurality of series-connected elementary switching circuits are grouped together.

Numerous advantages arise from the development of a single switching circuit and also from the construction of a switching matrix which is constituted by an array of these circuits. In the first place, the matrix involves the use of only one type of switching circuit, the location of these circuits is standard and a function which is written in its optimum form can easily be realized by unskilled personnel. By virtue of its analogy with a network of electrical contacts, the writing symbolism employed (binary analysis) does not require any complicated initiation and visualizes with maximum clarity the different functions which are included in a much larger assembly: these functions are all available in the matrix which also makes it possible to produce meshed (or branched) forms, parametric and iterative forms. Accordingly, this frequently results in an appreciable economy of switching circuits.

The matrix location of elementary switching circuits provides total freedom to modify a completed project at any moment, this flexibility being obtained neither at the expense of rapidity nor at the expense of reliability of operation. Furthermore, the dimensions of matrix

are always adaptable to the user's requirements by extension or subdivision. Its use is not limited to the combinatorial system (transcoding function) and its constructional design serves to carry out sequential operations while taking transient information into account; it also serves to produce time-delays whenever these latter prove necessary for a correct arrangement of sequences.

The overall cost price and the time of construction of an assembly can be accurately determined at the actual design stage since there is no expenditure or additional studying time to be added to the conditions of supply of the elementary switching circuits employed. Moreover, the simplicity of the matrix structure is a guarantee both of economy and reliability of operation.

The invention is not limited solely to the embodiments which have been illustrated and described by way of explanatory example but not in any limiting sense.

I claim:

1. A switching matrix for realizing at least one transcoding function having a constant switching time-delay between different binary variables, comprising an array of switching circuits which are all identical and disposed in the form of a matrix table having *n* lines and *m* columns, each circuit comprising an input terminal C proper of said circuit and an input terminal E of said applied binary variable, an output terminal L proper of said circuit and an auxiliary output terminal S which supplies the complemented value of the value which appears at said output terminal L proper, each succeeding circuit on a line of said matrix having an input C proper coupled to the output L proper of the preceeding circuit which is located on the same line and each preceeding circuit on a line of said matrix having an output L proper coupled to the input C proper of the succeeding circuit which is located on the same line, the inputs C proper of the circuits of the first column of said matrix being all connected to ground, means for providing selected connections between the different circuits through the intermediary of the terminals L, E and S, and means for applying said binary variables to said terminals E, the structure of each circuit being such as to have the following relations between the input and output values:

$$S = E \cdot \text{AND} \cdot \overline{C} \text{ and } L = \overline{S}.$$

2. A switching matrix according to claim **1,** wherein each circuit is constituted by a first transistor having a base coupled to the input E of the binary variable through a Zener diode, an emitter coupled to the output L proper, a first biasing resistor connected between said binary variable input E and a bias voltage source, a second transistor having a grounded emitter, a collector coupled to the auxiliary output S and a base connected through a Zener diode to the collector of said first transistor, and a second biasing resistor connected between said voltage source and the collector of said first transistor.

* * * * *