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(54) **METHOD FOR FABRICATING
ARRAY-MOLDED PACKAGE-ON-PACKAGE**

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257/E21.505**

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(57) **ABSTRACT**

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A method and apparatus for fabricating a semiconductor device are disclosed. The method attaches semiconductor chips (130) on a sheet-like insulating substrate (101) integral with two or more patterned layers of conductive lines and vias and with contact pads (103) in pad locations. A mold is provided, which has a top portion (210) with metal protrusions (202) at locations matching the pad locations. The protrusions are shaped as truncated cones of a height suitable to approach the pad metal surface in the closed mold cavity. The substrate and the chip are loaded onto the bottom mold portion (310); the mold is closed by clamping the top portion onto the bottom portion so that the protrusions are aligned with the contact pads, approaching the pad surface. After pressuring encapsulation compound into the cavity, the mold is opened; the encapsulated device has apertures to the pad locations. Any residual compound formed on the pads is removed by laser, plasma, or chemical to expose the metal surface.

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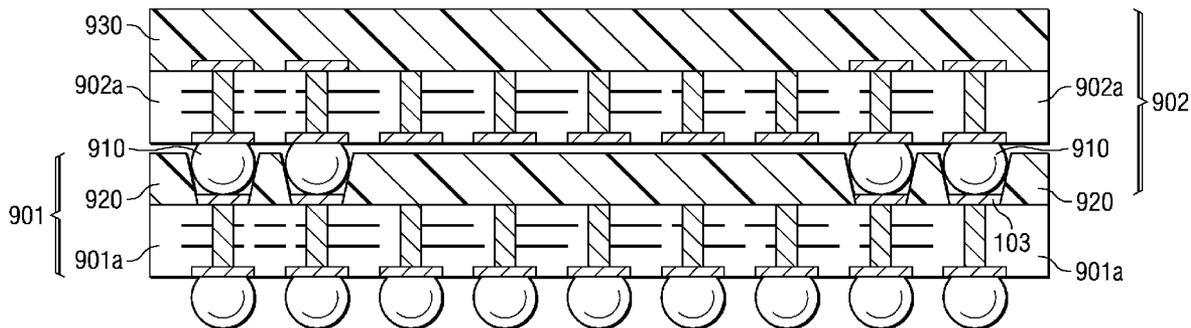




FIG. 2A

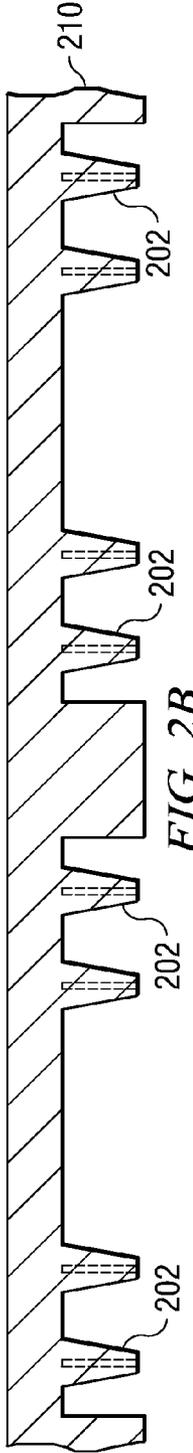


FIG. 2B

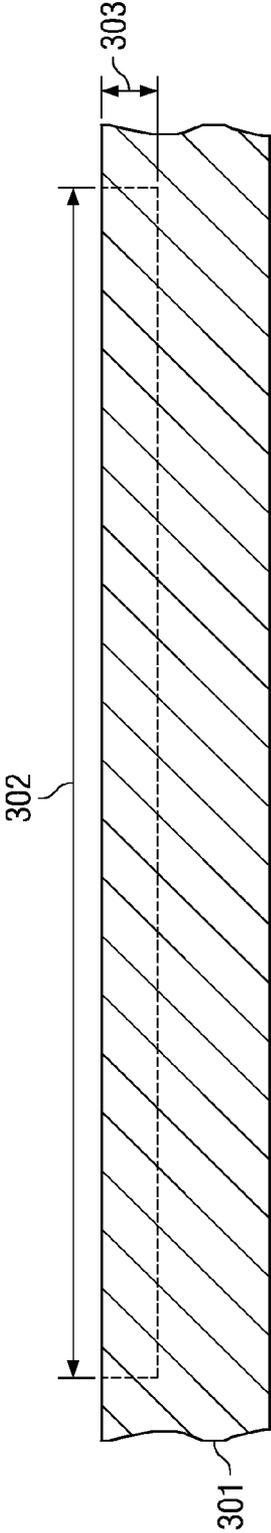


FIG. 3A

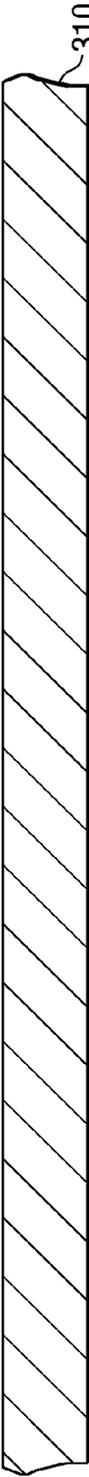


FIG. 3B

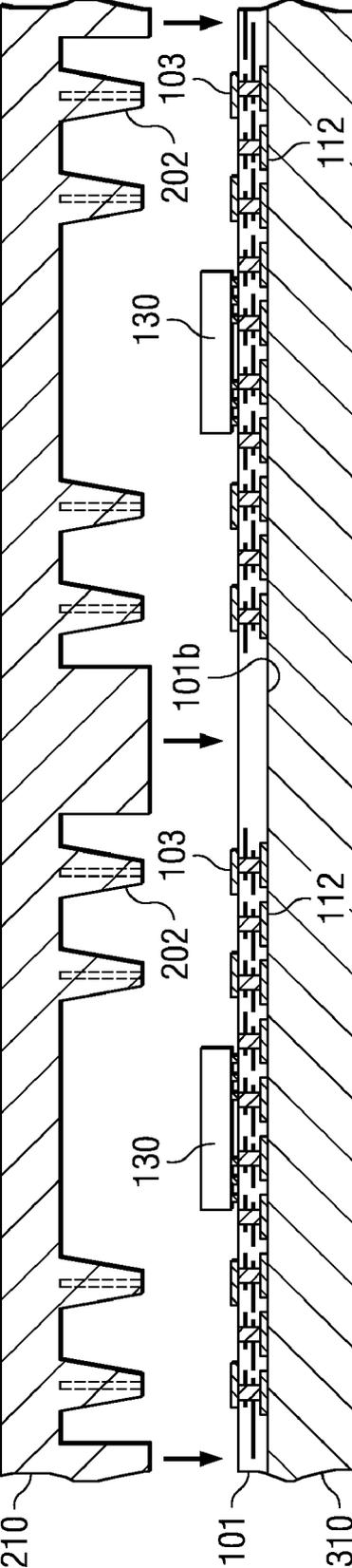


FIG. 4

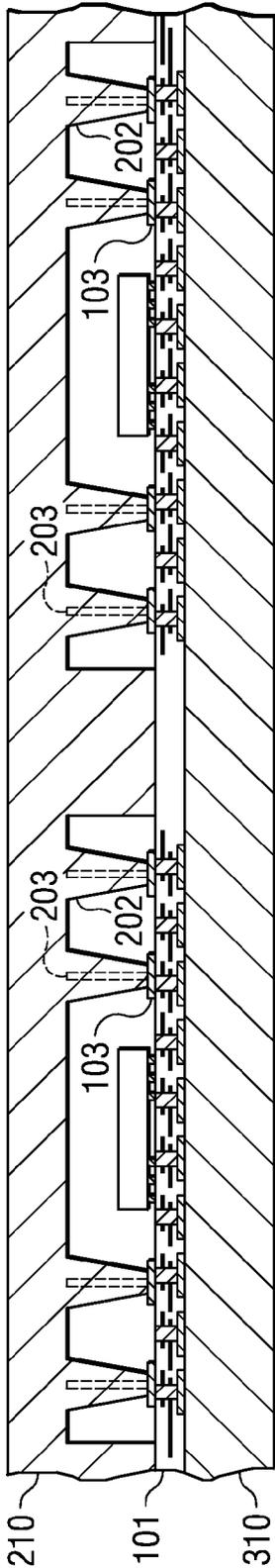


FIG. 5

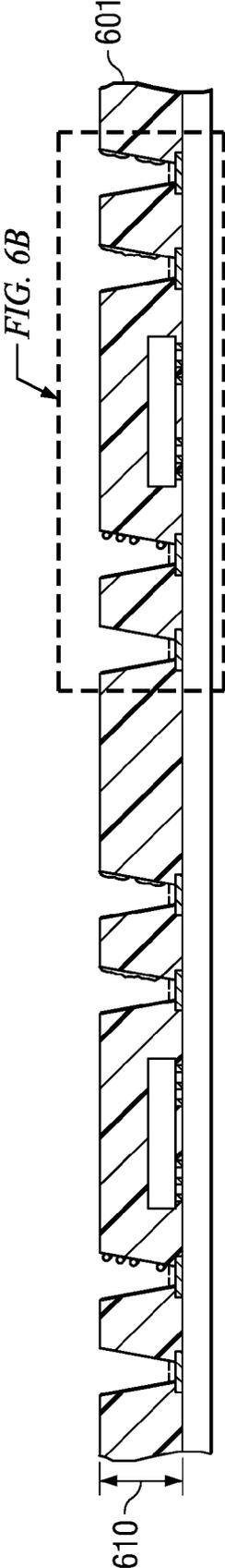


FIG. 6A

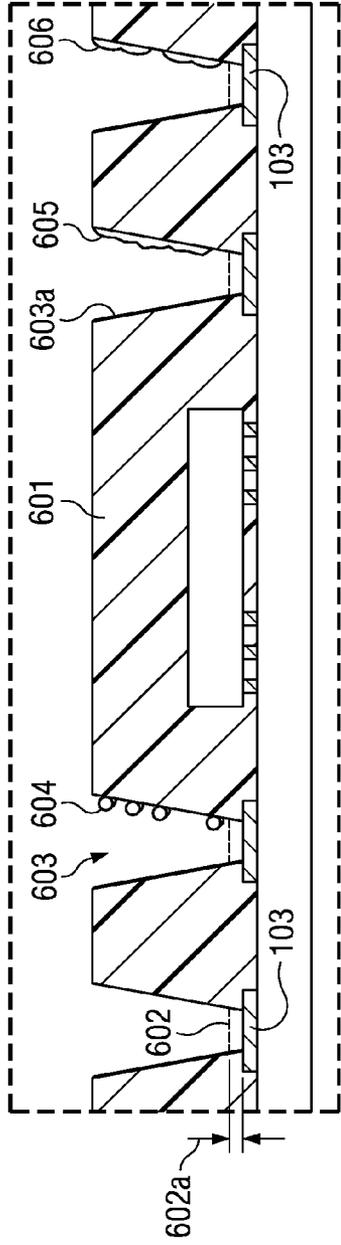


FIG. 6B

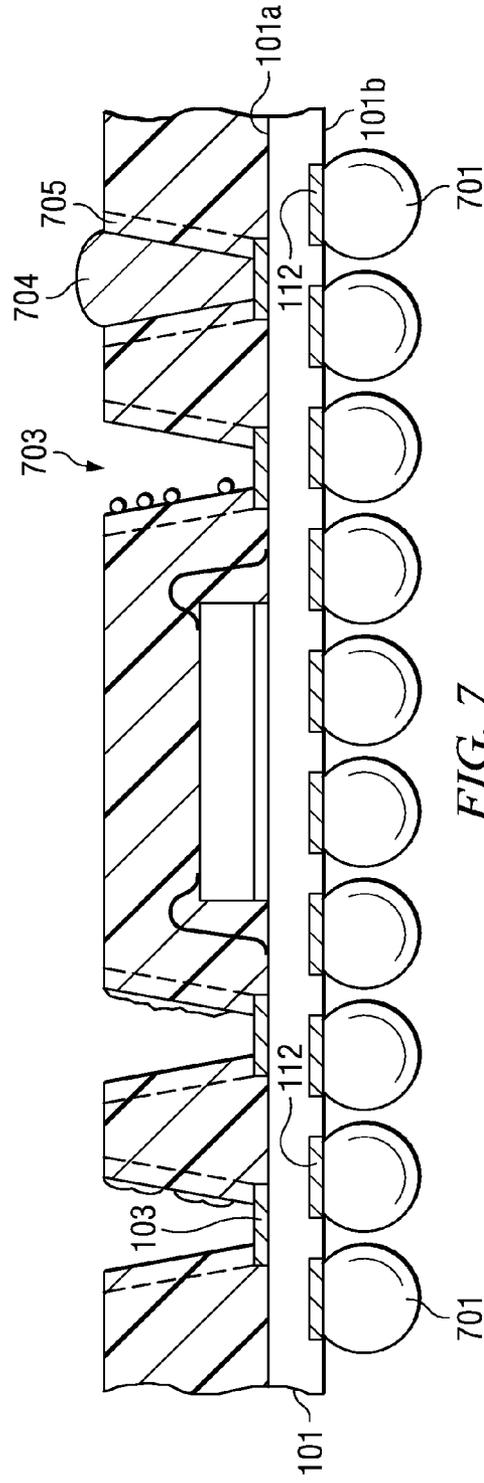


FIG. 7

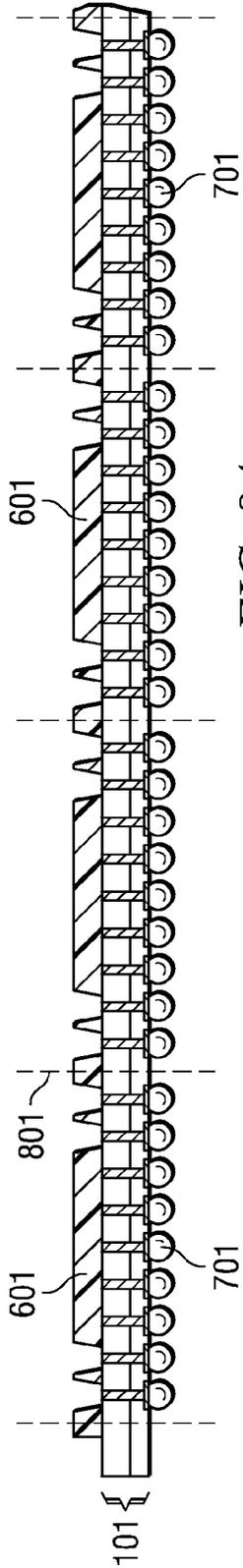


FIG. 8A

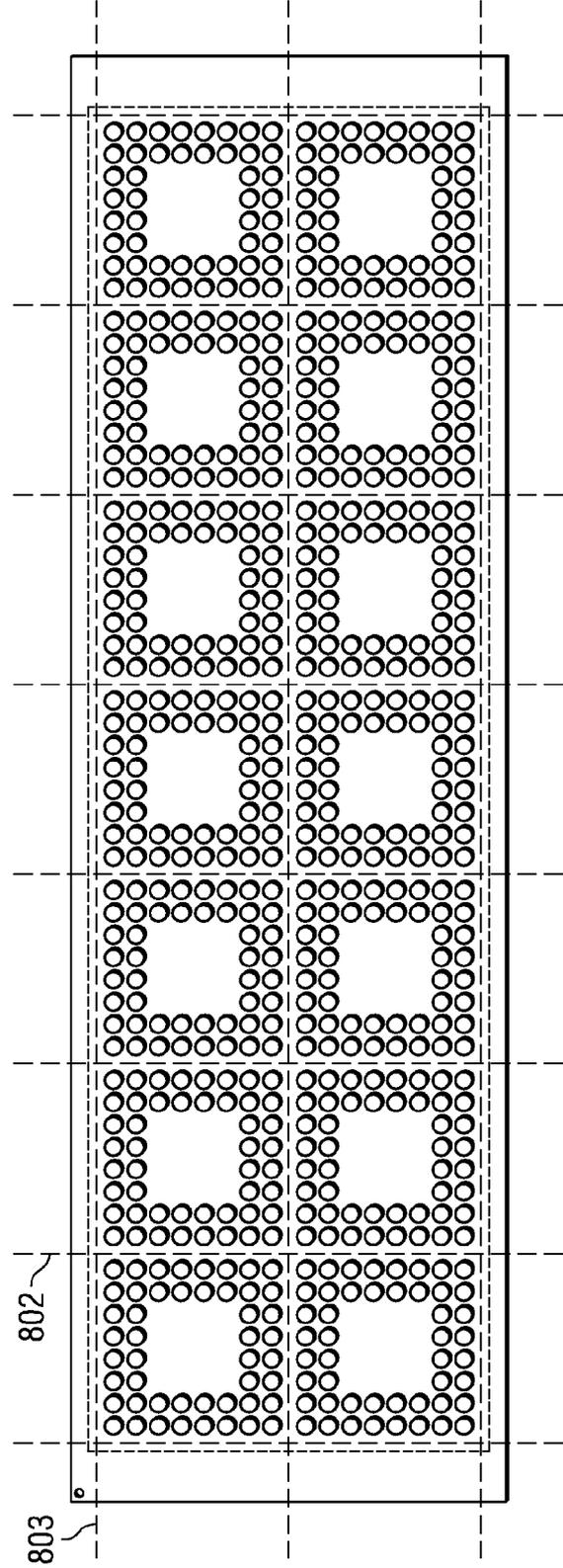


FIG. 8B

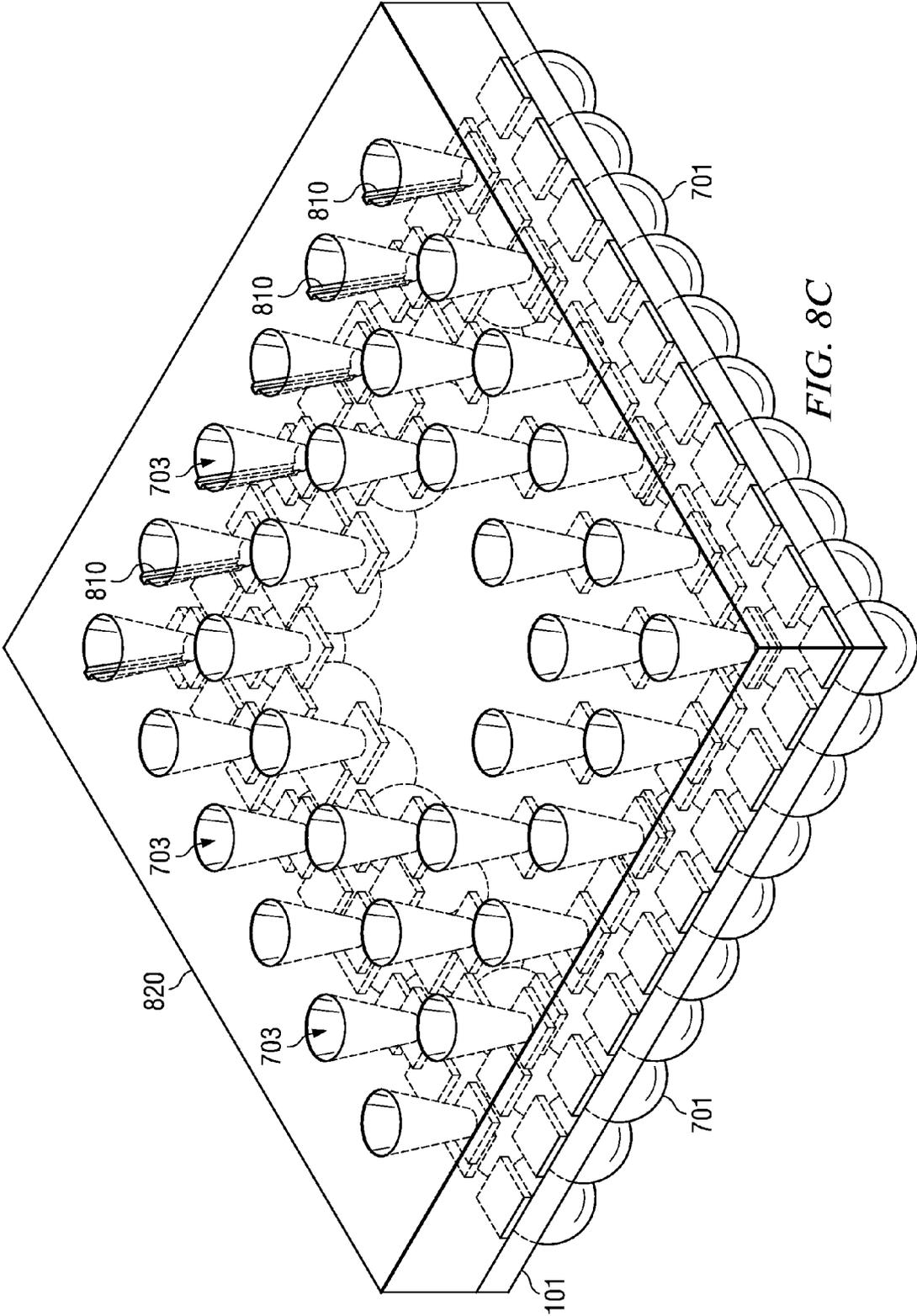


FIG. 8C

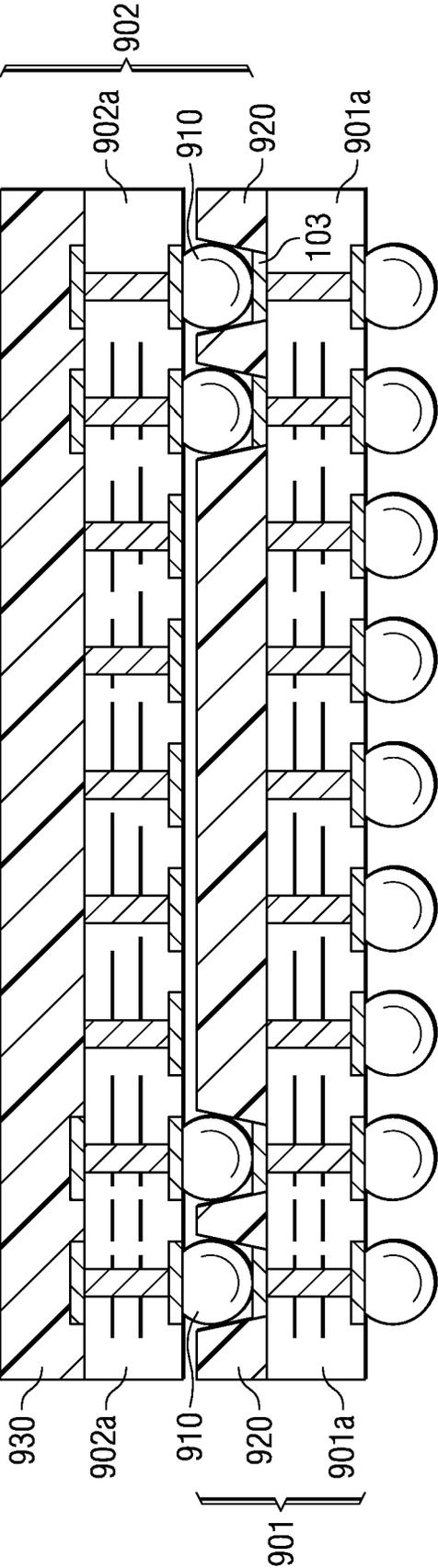


FIG. 9

**METHOD FOR FABRICATING
ARRAY-MOLDED PACKAGE-ON-PACKAGE**

FIELD OF THE INVENTION

[0001] The present invention is related in general to the field of semiconductor devices and processes and more specifically to the structure and fabrication method of low-profile, vertically integrated package-on-package integrated circuit assemblies.

DESCRIPTION OF THE RELATED ART

[0002] The thickness of today's semiconductor package-on-package products is the sum of the thicknesses of the semiconductor chips, electric interconnections, and encapsulations, which are used in the individual devices constituting the building-blocks of the products. This simple approach, however, is no longer acceptable for the recent applications especially for hand-held wireless equipments, since these applications place new, stringent constraints on the size and volume of semiconductor components used for these applications.

[0003] Furthermore, while the market place renewed a push to shrink semiconductor devices both in two and in three dimensions, the miniaturization effort included packaging strategies for thinner semiconductor devices as well as electronic systems. This trend to reduce product thickness initiated an increasing tendency to have product warpage problems, especially in thin assemblies, caused by the mismatch in the coefficients of thermal expansion (CTE) between the semiconductor chip, the plastic substrates, the molding compound, the solder balls, and the printed circuit board. For instance, with silicon as the semiconductor material and plastic FR-4 as substrate material, the difference in CTE is about an order of magnitude. Warpage is aggravated by repeated temperature cycles and solder reflows. Warpage can lead to some of the most debilitating problems encountered by semiconductor assemblies such as the fracture and separation of solder joints, or the separation of materials followed by moisture ingress.

SUMMARY OF THE INVENTION

[0004] Applicants recognize an existing need to shrink semiconductor devices both in two and in three dimensions, especially for a device-stacking and package-on-package method for semiconductor devices as well as electronic systems. Specifically, applicants recognize an existing need to design production equipment such as molds, to fabricate devices directly usable for assembling package-on-package the products.

[0005] The invention solves the problem by constructing one mold portion with contours so that the molded device will offer direct coupling with another device to form a package-on-package product. In addition, the new fabrication method is low-cost and simplified, and the products provide improved testability and thus yield. Using these contoured molds, stacking chips and packages will shorten the time-to-market of innovative products such as vertically integrated semiconductor systems, which utilize available chips of various capabilities (for example processors and memory chips), eliminating the wait for a redesign of chips.

[0006] Based on the contoured mold equipment, package-on-package devices can be produced with excellent electrical performance, mechanical stability free of warping, and high

product reliability. Further, it is a technical advantage that the fabrication method is flexible enough to be applied for different semiconductor product families and a wide spectrum of design and process variations.

[0007] One embodiment of the invention is a method for fabricating a semiconductor device. A semiconductor chip is assembled on a sheet-like insulating substrate integral with two or more patterned layers of conductive lines and conductive vias and contact pads in pad locations. A mold is provided, which has a top portion with metal protrusions at locations matching the pad locations; the protrusions are shaped as truncated cones of a height suitable to approach the pad metal surface in the closed mold cavity. The bottom mold portion is featureless. The substrate with the chip is loaded onto the bottom mold portion; the mold is closed by clamping the top portion onto the bottom portion so that the protrusions are aligned with the contact pads, approaching the pad surface. A cavity is thus formed by the top portion. After pressuring encapsulation compound into the cavity, the mold is opened. The encapsulation of the molded device has apertures to the pad locations. Finally, any residual compound formed on the pads is removed to expose the metal surface.

[0008] The protrusions approach the pad metal surface in the closed cavity to a distance between 0 and 100 μm. The compound formed in that distance can be removed either by shining laser light into the compound apertures, depositing compound particles on the sidewalls; or by a plasma clean-up process, leaving a roughened surface on the aperture sidewalls; or by a chemical etch process, leaving a compound undercut next to the pad metal surface.

[0009] The mold apertures may be filled with solder material contacting the pad metal surface, or they may serve to attach another semiconductor device with solder bodies, creating a package-on-package semiconductor assembly.

[0010] Another embodiment of the invention is a mold with top and bottom portions forming a cavity for holding semiconductor devices, wherein the device includes a semiconductor chip assembled on a sheet-like insulating substrate having contact pads in pad locations and with a metal surface. The mold is operable to be closed by clamping the top portion onto the bottom portion. The top portion includes metal protrusions at locations matching the pad locations; the protrusions are shaped as truncated cones of a height suitable to approach the pad metal surface in the closed cavity. The cones are angled with a range of about 10 to 30 degrees from vertical. Furthermore, the protrusions may optionally include a ridge operable to create a gas release channel in the aperture of the contact pads.

[0011] Another embodiment of the invention is a semiconductor device including a sheet-like insulating substrate with a perimeter, a first (top) surface with a chip assembly site and contact pads in pad locations and with a metal surface, and a second (bottom) surface. A semiconductor chip is assembled (by wire bonding or by flip-chip) on the assembly site. An encapsulated region, located only on the top substrate and extending to the substrate perimeter, encloses the chip in compound and has contact apertures at the pad locations for permitting external communication with the metal surfaces; the apertures may include sidewall surfaces with compound structures modified from its smooth-molded character by a metal clean-up process.

[0012] The compound structures on the aperture sidewalls may include thermally modified compound particles indicative of a laser process used for exposing the pad metal. Alter-

natively, the aperture sidewalls may have a roughened surface indicative of a plasma clean-up process used for exposing the pad metal. Or alternatively, the aperture sidewalls have indications of a chemical etch process used for exposing the pad metal.

[0013] The device further may have elongated grooves in the contact apertures operable as gas release channels. Solder material may be in the apertures, contacting the pad metal surface. Alternatively, another semiconductor device with solder balls can be attached to the first substrate surface by contacting the pad surfaces with the solder balls and thus creating a package-on-package semiconductor assembly. In addition, solder bodies may be attached to the second substrate surface.

[0014] The technical advances represented by certain embodiments of the invention will become apparent from the following description of the preferred embodiments of the invention, when considered in conjunction with the accompanying drawings and the novel features set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIGS. 1A to 7 illustrate certain process steps for fabricating an array-molded semiconductor device according to an embodiment of the invention.

[0016] FIG. 1A is a schematic cross section of a substrate with contact pads and a semiconductor chip assembled by wire bonding.

[0017] FIG. 1B is a schematic cross section of a substrate with contact pads and a semiconductor chip assembled by flip-chip technology.

[0018] FIG. 1C is a schematic cross section of a sheet-like substrate with contact pads and a plurality of chips flip-assembled for array processing.

[0019] FIG. 2A shows a schematic cross section of the top portion of a mold with structural features according to the invention.

[0020] FIG. 2B shows a schematic cross section of the top portion of a mold intended for array-molding with structural features according to the invention.

[0021] FIG. 3A shows a schematic cross section of the bottom portion of a mold.

[0022] FIG. 3B shows a schematic cross section of the bottom portion of a mold intended for array-molding.

[0023] FIG. 4 illustrates a schematic cross section of the open mold according to an embodiment of the invention, loaded with a substrate assembled with semiconductor devices.

[0024] FIG. 5 shows a schematic cross section of the closed mold according to an embodiment of the invention, loaded with a substrate assembled with semiconductor devices.

[0025] FIG. 6A illustrates a schematic cross section of a molded semiconductor array after removal from the mold.

[0026] FIG. 6B shows a magnified schematic cross section of a molded unit after removal from the mold and singulation from the array.

[0027] FIG. 7 is a schematic cross section of a discrete device after removing any molding compound from the contact pads, filling an aperture with solder, and attaching solder bodies for external communication.

[0028] FIG. 8A shows a schematic cross section of a finished array with features according to the invention.

[0029] FIG. 8B depicts a schematic top view of a finished array, molded according to the invention, before singulation.

[0030] FIG. 8C shows a schematic perspective view of a discrete unit singulated from the molded array with features according to the invention.

[0031] FIG. 9 illustrates a schematic cross section of another embodiment of the invention, wherein a second semiconductor device with solder bodies is attached to the first device so that the aperture-exposed pads of the first device are contacted by the solder bodies of the second device, creating a package-on-package semiconductor assembly.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0032] FIGS. 1A through 7 illustrate schematically the steps of one embodiment of the present invention, a method for array-molding semiconductor devices. The steps shown in FIGS. 1A and 1B show the assembly of a semiconductor chip on a substrate by wire bonding (FIG. 1A) and by flip-chip technology (FIG. 1B); FIG. 1C exemplifies a portion of an array of chips assembled by flip-chip. A sheet-like substrate 101 with insulating core (for example, plastic, glass-fiber reinforced, ceramic) is integral with two or more patterned layers of conductive lines and conductive vias (preferably copper) and contact pads in pad locations. Lines 110 do not reach beyond the boundaries of substrate 101. Substrate 101 has a first surface 101a and a second surface 101b, and a preferred thickness range from 0.2 to 0.5 mm. The first surface 101a includes chip assembly sites 102 and contact pads 103 in pad locations. The metal of the contact pads is preferably copper with a solderable surface (for example, including a layer of gold or palladium). Second surface 101b also has pads 112 with a solderable surface.

[0033] A plurality of semiconductor chips 130 is provided. In order to attach and electrically connect the chips, they are assembled on each assembly site either by adhesive attachment and wire bonding, or by flip-chip connection. For flip-attachment, the connecting metal bumps 140 may be made of solder, gold, or copper.

[0034] As illustrated in FIG. 2A to 3B, in the next process step a mold made of steel or another suitable material is provided, which allows the encapsulation of a single unit or an array of units. The mold has a top portion manufactured to include recesses suitable for a cavity, and a bottom portion; when closed, the mold is forming a cavity for holding semiconductor devices. In FIG. 2A, the top portion is intended to process a single unit and is designated 201; in FIG. 2B, the top portion is constructed for an array of units to be processed together as a batch. In FIG. 3A, the bottom portion is intended to process a single unit and is designated 301; in FIG. 2B, the bottom portion is constructed for an array of units to be processed together.

[0035] The top portion 201 includes protrusions 202 at locations matching the pad locations of the device shown in FIGS. 1A and 1B; the bottom portion 301 is without corresponding protrusions. The protrusions are preferably shaped as truncated cones, with the cone surface angled within a preferred range from about 10 to 30 degrees from vertical. The angle is designated 202a in FIG. 2A. Furthermore, the protrusions preferably may have a ridge 203, which may extend along the whole angled side of the cone. Ridge 203 is operable to create a groove or channel in the molded part, which may provide release of gas in the solder ball attachment process, or help in the solder paste reflow process.

[0036] The height 202b of the protrusion is selected to be suitable to approach the substrate pad metal (103 in FIGS. 1A

and 1B) in the closed mold. Preferably, the protrusion should approach the pad metal surface in the closed mold to a distance between 0 and about 100 μm . More preferably, height 202b of the protrusion is sufficient to touch the pad metal surface in the closed mold.

[0037] The bottom portion 301 in FIGS. 3A and 310 in FIG. 3B of the mold has no protrusions; it is featureless and preferably flat. For some individual devices, it may be an advantage to recess a portion outlined by length 302 and depth 303 sufficient to accommodate the substrate of a discrete device, but for array processing, a featureless flat bottom mold portion is preferable.

[0038] In the next process step (see FIG. 4), the substrate 101 with the assembled chips 130 is loaded onto the bottom mold portion 310. The second substrate surface 101b is rested on mold portion 310, and the first substrate surface 101a with the contact pads 103 is positioned away from the bottom mold portion 310. Protrusions 202 of the top mold portion 210 are aligned with the respective contact pads 103 of substrate 101.

[0039] FIG. 5 shows the next process step of closing the mold by clamping the top portion 210 onto the bottom portion 310 so that the protrusions 202 are aligned with the contact pads 103, approaching or touching the pad surface. The top portion 210 resting on the flat bottom portion 310 forms the cavity of the mold for holding the semiconductor devices. Preferably, the protrusions touch the contact pads; however, material or alignment tolerances may cause a residual distance between 0 and about 100 μm between the protrusion and the pad. FIG. 5 also shows the respective ridge 203 for each protrusion 202.

[0040] In order to avoid any residual distance between protrusions and pads, causing a gap between protrusions and pads, and thus to avoid any bleeding of mold compound into the gap, an alternative method includes the step of placing a thin sheet 220 of compliant, inert polymer over the surface 201a of the complete top mold portion (see FIG. 2A). The polymer is selected to tolerate significant pressure from the protrusions clamped against the pads. The sheet may have a chemical composition to be either dissolved into the molding compound and become part of the molded encapsulation, or, preferably, remain a coherent sheet which can be readily peeled off the top mold portion, after the mold is opened again.

[0041] Next, encapsulation material such as epoxy-based and filler-loaded molding compound is pressured into the cavity to fill the cavity; the runners for supplying the compound, and the gates needed for entering the cavity and controlling the compound flow, are not shown in FIG. 5. By this transfer molding step, encapsulations for the devices of the array are created.

[0042] After partially polymerizing the compound 601, the mold is opened and the substrate together with the encapsulated array of chips is removed from the mold; FIG. 6A illustrates the encapsulated array, and FIG. 6B shows an enlarged view of one unit. Subsequently, compound 601 is fully polymerized. For many device types, the thickness of the molded encapsulation is between 0.6 and 0.7 mm. FIGS. 6A and 6B show that the encapsulation has apertures 603 to the pad locations.

[0043] FIG. 6B indicates by dashed contour 602 any residual encapsulation that may form on the contact pads 103. These thin deposits (thickness 602a between 0 and about 100 μm), if formed, have to be removed to expose the clean metal

surface of pad 103. At least three methods are suitable to remove these unwanted encapsulation layers.

[0044] The first method employs drilling or vaporizing by laser light. A focused laser beam shines into the encapsulation aperture 603, removes the compound layer thereby forming particles 604 in a thermal process, and may deposit these particles on the otherwise smooth sidewalls 603a; particles 604 attest to the thermal process used to clean up the pads. The second method employs a plasma clean-up process; the plasma leaves a roughened surface 605 on the aperture sidewalls 603a. The third method employs a chemical etch process, which leaves a surface structure 606 recognizable by one skilled in the art. All three methods are material-sensitive and thus controllable to stop at the metal surface of the contact pads.

[0045] When the compliant inert film is employed, which can be peeled off after the molding process (see above), the pad metal surfaces remain clean throughout the molding process and consequently no clean-up step is necessary.

[0046] In an additional process step, reflow bodies such as solder balls 701 are attached to the attachment pads 112 (see FIGS. 1A and 1B) on the second substrate surface 101b. This step is illustrated in FIG. 7, showing a magnified portion of the array (it should be noted that in the example of FIG. 7, wire bonding has been employed to assemble the chip on the first substrate surface 101a).

[0047] In an optional process step, the mold apertures 703 may be filled with solder paste 704, which contacts the surface of pad metal 103. During the reflow step of the paste, grooves 705 may help to separate the flux-rich part from the solder-rich part.

[0048] FIGS. 8A, 8B, and 8C depict the singulation step. The dashed lines 801 (in the cross section of FIG. 8A), 802 and 803 (in the top view of FIG. 8B) indicate saw lines of saws, which cut through the mold compound 601 and the substrate 101 to singulate discrete units from the sheet-like substrate of the array. Due to the sawing process step, the individual units have recognizable saw marks on their sides.

[0049] A discrete unit is illustrated in FIG. 8C in an X-ray view, which emphasizes the apertures 703 to the contact pads, but omits the encapsulated assembled chip for clarity reasons (not to scale). In addition, the gas release channels 810 have been omitted for all apertures except for one row of apertures.

[0050] The gas release channels help to prevent the trapping of air and gas, when another device 902 with solder bodies 910 is attached to the first device 901 and the apertures are filled with solder to contact the exposed surfaces of the contact pads 103. FIG. 9 illustrates a resulting package-on-package semiconductor assembly.

[0051] Another embodiment of the invention is an apparatus for the fabrication of a semiconductor device; the apparatus is illustrated in FIGS. 2B and 3B. A mold has top (201 in FIG. 2A, 210 in FIG. 2B) and bottom (301 in FIG. 3A, 310 in FIG. 3B) portions; the top portion has a cavity with protrusions for holding semiconductor devices, the bottom portion is without corresponding protrusions and preferably featureless. Preferably, the device includes a semiconductor chip attached to a sheet-like insulating substrate with contact pads in pad locations. When the mold is operated, it is closed by clamping the top portion onto the bottom portion, whereby a cavity is formed.

[0052] The top portion includes protrusions (202 in FIG. 2A) at locations matching the pad locations. Preferably, the protrusions are made of the same material (for instance, steel)

as the top portion of the mold. The protrusions are preferably shaped as truncated cones of a height suitable to approach the pad metal surface in the closed mold; a practical distance from the cone to the pad surface is between 0 and about 100 μm . More preferably, the height is suitable to touch the pads metal surface in the closed mold. The angle $202a$ of the cones is preferably between 10 and 30 degrees from vertical. In addition, it is advantageous to add a ridge to the protrusions (203 in FIG. 2A), which are configured to create, in the molded encapsulation, a gas release channel in the aperture of the contact pads. The release channel provides an escape for air and other gases in the solder attachment process, when the aperture is being filled with solder.

[0053] The bottom portion of the mold is preferably featureless, in particular in molds for encapsulating whole arrays as shown in FIG. 3B. The bottom part provides support for placing the device substrate in the mold. On the other hand, it may be advantageous for molding discrete devices to have a recess (302 in FIG. 3A) of a certain depth in the bottom part for tightly positioning the device substrate. No molding compound reaches the bottom of the cavity or the bottom surface of the substrate.

[0054] Another embodiment of the invention is a semiconductor device, singulated by sawing from an array-molded substrate, and designed to become part of a semiconductor package-on-package device. An example of the embodiment is illustrated in FIG. 8C; a magnified cross section before singulation is depicted in FIG. 7. A sheet-like insulating substrate 101 has obtained its perimeter 820, preferably by sawing, which leaves recognizable saw marks. The substrate has a first surface 101a with a chip assembly site and contact pads 103 in pad locations and with a metal surface. The substrate further has a second surface 101b with attachment sites for solder bodies 701.

[0055] A semiconductor chip is attached to the assembly site (not shown in FIG. 8C); the attachment and assembly may be performed by wire bonding, as depicted in the example of FIG. 7, or by flip-chip technology, shown in FIG. 6B.

[0056] The embodiment has an encapsulated region, only on the top of the substrate and defined by the substrate perimeter 820. Consequently, the encapsulation material covers the whole top substrate area of the device, including the chip. The encapsulation forms contact apertures 703 at the pad locations for permitting external communication with the pad metal surfaces 103; preferably, the apertures have the shape of cones. The surfaces of the aperture sidewalls include compound structures, which have been modified from the otherwise smooth surface by the process employed to clean up the pad metal surfaces and thus bear witness of the selected process.

[0057] As an example, when the compound structures on the sidewalls include thermally modified compound particles, such as rounded particles, they indicate that a laser technique has been used to remove an incidental compound layer from the pad surface and thus expose the pad metal.

[0058] Alternatively, when the aperture sidewalls have a roughened surface, they indicate that a plasma clean-up process has been used to expose the pad metal.

[0059] In another situation, the aperture sidewalls may have surface structures recognizable by one skilled in the art as residues of a chemical etch process used to expose the pad metal.

[0060] In one row of apertures, FIG. 8C depicts elongated grooves in the contact apertures operable as gas release chan-

nels. While allowing trapped gas to escape in the process of reflowing a solder ball in the aperture, these grooves may end up being filled with solder. The support function is especially beneficial during the process step of attaching another semiconductor device 902 with solder bodies 910 to the first substrate surface of the first device 901 in order to produce a package-on-package semiconductor product as shown in FIG. 9. In this attachment process, the pad surfaces 103 are contacted by the solder bodies 910 of the second device 902, creating the package-on-package assembly. FIG. 9 stresses the preferred combination of devices, wherein not only the molding compound 920 of first device 901 extends to the substrate perimeter 901a, but also the molding compound 930 of second device 902 extends to the substrate perimeter 902a. This combination minimizes the risk of device warpage in the assembly process.

[0061] While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the invention applies to products using any type of semiconductor chip, discrete or integrated circuit, and the material of the semiconductor chip may comprise silicon, silicon germanium, gallium arsenide, or any other semiconductor or compound material used in integrated circuit manufacturing.

[0062] As another example, the metal protrusions of the top mold portion may be shaped as cylinders, cubes, rhomboids, or any other 3-dimensional configuration. It is therefore intended that the appended claims encompass any such modifications or embodiment.

We claim:

1. A method for fabricating a semiconductor device comprising the steps of:
 - providing a sheet-like insulating substrate integral with two or more patterned layers of conductive lines and vias, the substrate having a first surface with chip assembly sites and contact pads in pad locations, and a second surface;
 - providing semiconductor chips;
 - attaching a chip to each assembly site;
 - providing a mold having top and bottom portions, the top portion forming a cavity for holding semiconductor devices;
 - the top portion including protrusions at locations matching the pad locations, the protrusions shaped as truncated cones of a height suitable to approach the pad metal surface when the mold is in a closed form;
 - the bottom portion being without corresponding protrusions;
 - loading the substrate with the chips onto the bottom mold portion, resting the second substrate surface on the mold and positioning the first surface with the contact pads away from the bottom mold portion;
 - closing the mold by clamping the top portion onto the bottom portion so that the protrusions are aligned with the contact pads, approaching the pad surface;
 - pressuring molding compound into the cavity to fill the cavity, thereby creating an encapsulation;
 - opening the mold and removing the substrate together with the encapsulated chips from the mold, the encapsulation having apertures to the pad locations; and

- removing any residual compound on the pads to expose the metal surface.
- 2. The method according to claim 1 wherein the protrusions approach the pad metal surface in the closed cavity to a distance between 0 and 100 μm.
- 3. The method according to claim 1 wherein the protrusion touches the pad metal surface in the closed mold.
- 4. The method according to claim 1 wherein the metal protrusions further include a ridge operable to create an aperture having a gas release channel in the aperture.
- 5. The method according to claim 1 wherein the step of removing residual compound from the pad surface is performed by the process of shining laser light into the encapsulation apertures, thereby depositing compound particles on the otherwise smooth sidewalls.
- 6. The method according to claim 1 wherein the step of removing residual compound from the pad surface is performed by a plasma clean-up process, thereby creating a roughened surface on the aperture sidewalls.
- 7. The method according to claim 1 wherein the step of removing residual compound from the pad surface is performed by a chemical etch process, thereby leaving etch structures on the aperture sidewalls.
- 8. The method according to claim 1 further including, before the step of loading the substrate, the step of placing a compliant film over the top portion loaded with the inserts.
- 9. The method according to claim 8 further including, after the step of opening the mold, the step of peeling the compliant film off the top portion.
- 10. The method according to claim 1 wherein the step of attaching the chip includes wire bonding.
- 11. The method according to claim 1 wherein the step of attaching the chip includes a flip-chip process.
- 12. The method according to claim 1 further including the step of attaching solder balls to the second substrate surface.
- 13. The method according to claim 1 further including the step of filling the encapsulation apertures to the pads with solder material.
- 14. The method according to claim 1 further including the step of singulating individual units from the sheet-like substrate.
- 15. The method according to claim 14 wherein the step of singulating is performed by a sawing process, thereby creating a surface with saw marks.
- 16. The method according to claim 15 further including the step of attaching another semiconductor device with solder balls to the first substrate surface of the singulated unit so that

- the exposed pad surfaces are contacted by the solder balls, thereby creating a package-on-package semiconductor assembly.
- 17. The method according to claim 1 wherein the pad metal surface has a layer including gold or palladium.
- 18. An apparatus for the fabrication of a semiconductor device comprising:
 - a mold having top and bottom portions, the top portion having a cavity for holding semiconductor devices, the device includes a semiconductor chip attached to a sheet-like insulating substrate integral with two or more patterned layers of conductive lines and vias, the substrate having contact pads in pad locations;
 - the mold operable to be closed by clamping the top portion onto the bottom portion;
 - the top portion including protrusions at locations matching the pad locations, the protrusions shaped as truncated cones of a height suitable to approach the pad metal surface in the closed mold; and
 - the bottom portion being without corresponding protrusions.
- 19. A device comprising:
 - a sheet-like insulating substrate integral with two or more patterned layers of conductive lines and vias, the substrate having a first surface with a chip assembly site and contact pads in pad locations, and a second surface;
 - a semiconductor chip attached to the assembly site; and
 - an encapsulated region on the first surface, extending to the edge of the substrate, enclosing the chip and having contact apertures at the pad locations for external communication with the metal surfaces, the apertures having a not-smooth sidewall surfaces.
- 20. The device according to claim 19 wherein the not-smooth aperture sidewall surfaces include laser spalled compound particles.
- 21. The device according to claim 19 wherein the not-smooth aperture sidewalls include a plasma-roughened surface.
- 22. The device according to claim 19 wherein the not-smooth aperture sidewall surfaces have chemically etched structures.
- 23. The device according to claim 19 wherein the semiconductor chip is attached to the substrate by wire bonding.
- 24. The device according to claim 19 wherein the semiconductor chip is attached on the substrate by a flip-chip process.

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