

FIG.1

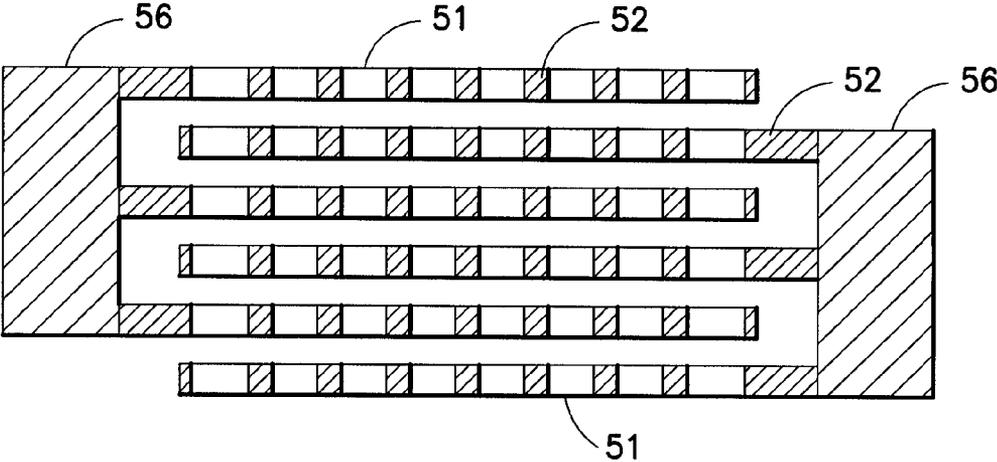


FIG.2

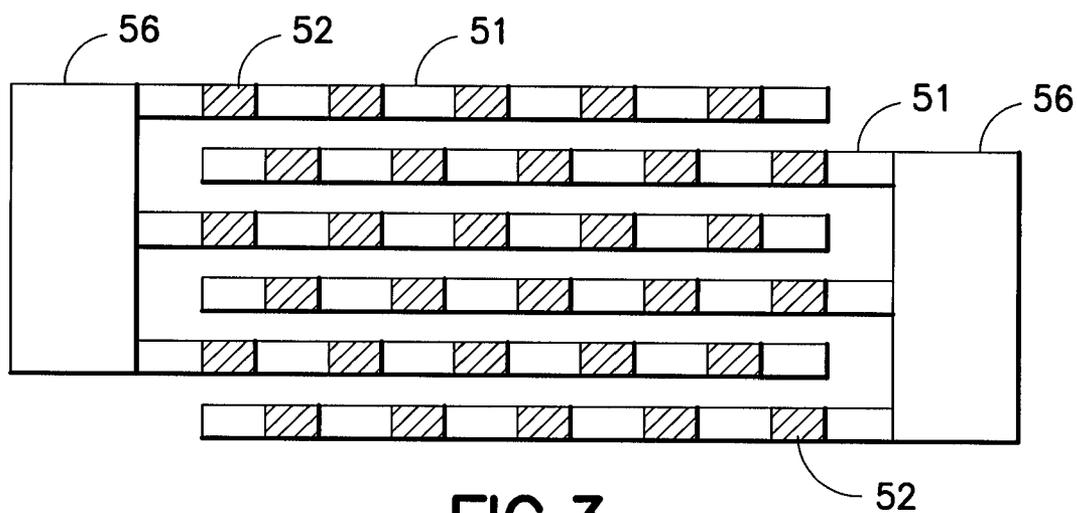


FIG. 3

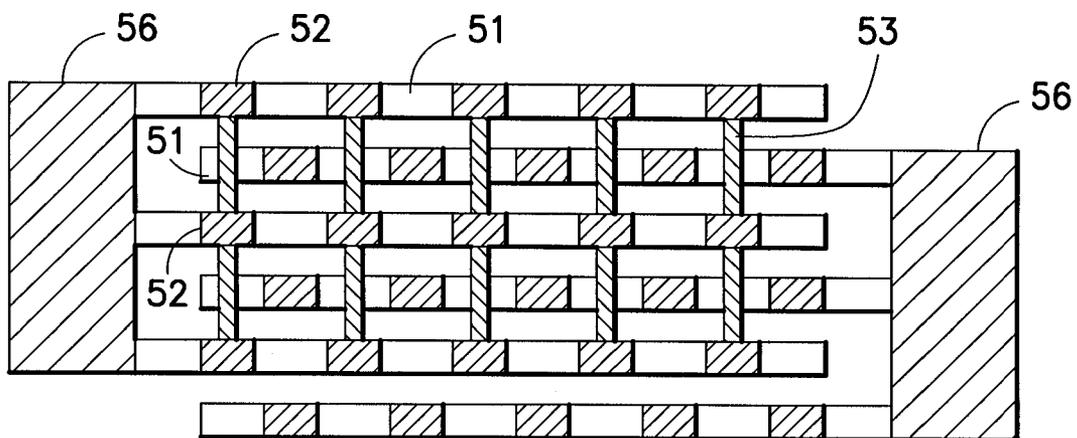


FIG. 4

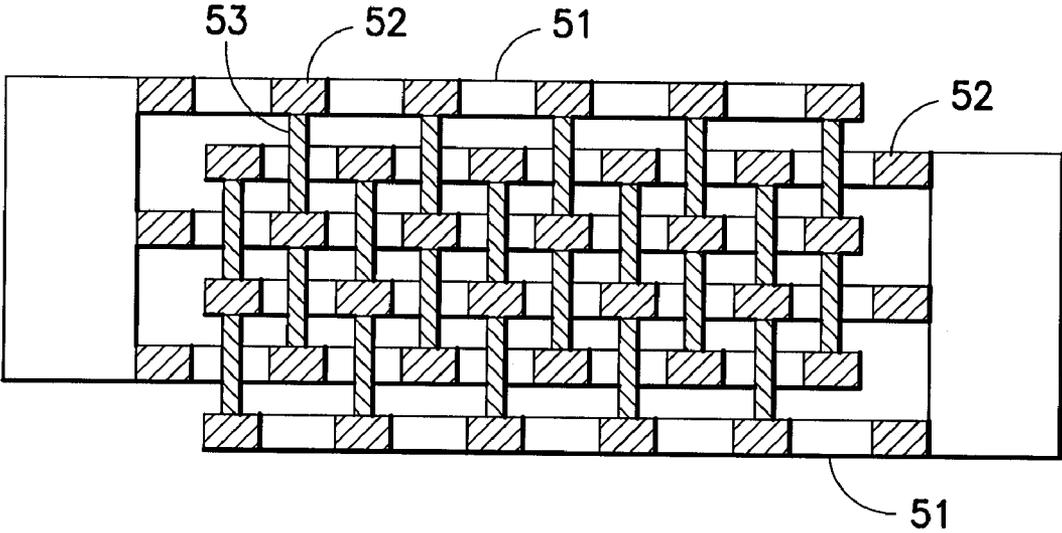


FIG. 5

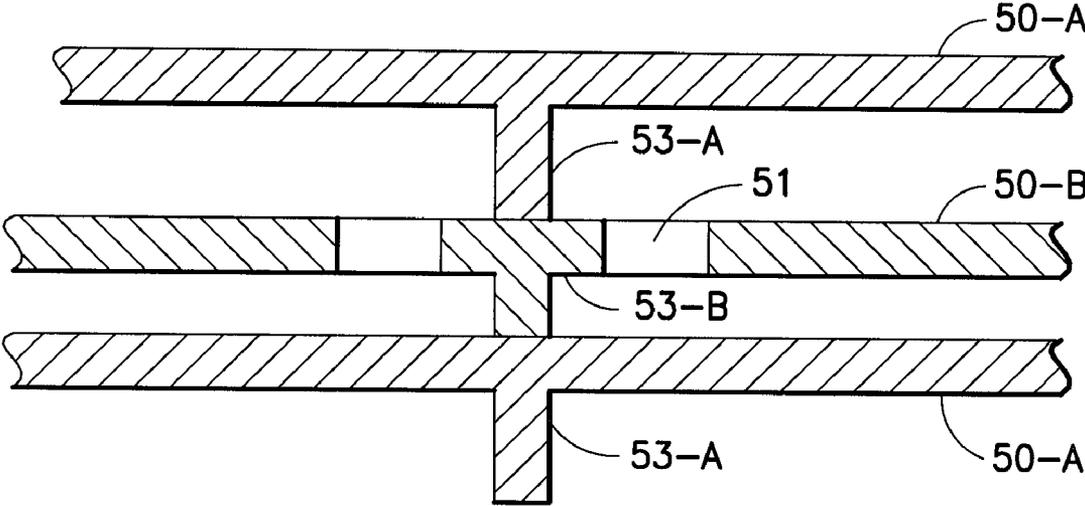


FIG. 6

INTEGRATED PARALLEL PLATE CAPACITORS

TECHNICAL FIELD

[0001] The field of the invention is that of forming a plate capacitor having a set of horizontal conductive plates separated by a dielectric (MIM-CAP).

BACKGROUND OF THE INVENTION

[0002] High performance (high Q-value) metal-insulator-metal capacitor (MIM cap) is one of the essential passive devices in RF/Analog circuitry. In order to achieve high-Q value, low resistance metal plates are typically used. In prior work, the bottom plate of a metal-insulator-metal (MIM) capacitor is typically made of back end of the line (BEOL) aluminum metal wire on the xth level of the back end (zero-cost). An additional photolithography mask is used for MIM cap top plate formation. This additional top plate mask leads to extra wafer processing cost of about \$25/wafer. In the advanced CMOS technologies with Cu BEOL, up to three masks are employed to create high-Q MIM capacitors.

[0003] In an effort to reduce cost, vertical parallel plate capacitors (VPP) have been recently developed/introduced in the advanced Analog/RF CMOS technologies. VPPs capacitor plates are made of BEOL Mx wire fingers and vias. Due to scaling of BEOL wiring width and spacing, the capacitance density of VPP becomes appreciable for technologies with minimum features smaller than 0.25 um. However, the performance of a VPP capacitor is limited because of the high resistance associated with metal fingers/vias, which is particularly troublesome for high frequency application.

[0004] As a result, a high performance MIM capacitor is still desirable & needed for Analog/RF CMOS technologies.

SUMMARY OF THE INVENTION

[0005] The present invention utilizes BEOL wide Cu planes as MIM capacitor electrodes and the existing inter-level dielectric layers as MIM dielectric films; i.e. the thickness of the capacitor plates and of the dielectric is the same in the capacitor as in the rest of the circuit.

[0006] The Mx electrodes are tied together to create a parallel plate capacitor. As a result, the resistance of MIM plates according to the present invention is extremely low, which leads to a high performance MIM capacitor.

[0007] The capacitance density for the invented MIM increases as the inter-level dielectric films become thinner for more advanced technologies. Moreover, more BEOL metal wiring levels are employed for advanced technologies, which can lead to higher capacitance density for the present invention because more metal levels can be connected together.

[0008] To further enhance capacitance density of this zero-cost high-Q MIM capacitor, Vx vias are added through Mx perforation holes (through-vias). The use of through-vias increases capacitive coupling and reduces/eliminates additional wiring area needed for MIM cap plate connection, which again leads to cap density enhancement.

[0009] An Ansoft Q3D simulation indicates that capacitance density improvement of greater than 30% is possible compared with through-via practice.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 shows a cross sectional view of a MIM-Cap with solid plates in the capacitor.

[0011] FIG. 2 shows cross sectional view of the same set of plates having perforations.

[0012] FIG. 3 shows the plates of FIG. 2 with the holes offset.

[0013] FIG. 4 shows the plates with the plates of one polarity being connected by vertical conductors.

[0014] FIG. 5 shows the plates with vertical connectors connecting all the plates of each polarity.

[0015] FIG. 6 shows a detail of the connection between vertical connectors on adjacent levels.

DETAILED DESCRIPTION

[0016] FIG. 1 shows a set of solid plates 50 connected alternately by vertical connection bars 56. An important feature of this structure compared with prior MIM capacitors is that the thickness 12 of the dielectric between the plates is greater than before because the thickness 12 is the thickness 16 of the back end levels minus the thickness 14 of the interconnects on that back end level; e.g. if the total thickness of the level is 0.5 microns and the thickness of the interconnect on that level is 0.25 microns, then the thickness 12 of the dielectric is also 0.25 microns. Dashed line 10 indicates the top surface of a layer in the back end. A level in the back end containing a capacitor plate will be referred to as a capacitor level. The foregoing means that the capacitance per unit area (capacitance density) is reduced, but that is more than compensated for by the improved reliability provided by the invention. Box 5 represents schematically interconnections on the levels of the BEOL and the remainder of the integrated circuit.

[0017] Fabrication of the invented high-Q MIM is fully compatible with Cu BEOL processing. The plates are deposited in apertures in the interlevel dielectric simultaneously with the other interconnects on that level. The blocks labeled 56 that connect the plates of each polarity are schematic representations. They may be vertical bars of metal, vertically aligned damascene conductors, regular interconnects, or any other structure. Preferably, they are vertically aligned dual damascene structures, so that no additional masks or processing steps are needed. No additional processing steps are added in this invented high-Q MIM. An estimate of the capacitance density for six levels of thin metal wire BEOL in 65 nm technology results in cap density of 0.88 fF/ μm^2 when no perforation is assumed.

[0018] This no perforation assumption is valid for MIMs that require small plates. When MIM plates become large (approximately 20 microns on edge), perforating of copper plates is necessary in order to achieve uniform copper plate thickness. Significant copper plate thinning is expected when large non-perforated Cu plates are used due to the fast Cu polish rate associated with large plates during CMP processing.

[0019] However, the capacitance density loss due to perforation is limited. Based on an Ansoft Q3D simulation using design information for a known process using 90 nm ground rules, the loss of capacitance density from perfora-

tion is only about 1/3 of the perforation density (for example, the capacitance reduction comparing 38% perforation to no perforation is only 11.5%).

[0020] FIG. 2 shows the same plates, illustratively having an area 30 micron² while the overlap area is 25 micron², with the addition of a set of holes 51 that are aligned vertically in each plate, regardless of polarity. The holes 51 are separated by solid portions 52 of the plates. Illustratively, the overlap area of the plates of the two polarities is 25 microns² and the 30 holes are 0.42 microns by 0.42 microns. The local hole density is 17.6%.

[0021] FIG. 3 shows an alternative version in which the holes on alternate plates are staggered, so that a hole 51 on a plate of one polarity is aligned vertically with a solid portion 52 of the plate immediately above and below.

[0022] FIG. 4 shows the same hole arrangement as FIG. 3, but with the addition of 0.14x0.14 micron vertical conductive members (vias) 53 connecting vertically one polarity of plates, whether positive or negative.

[0023] FIG. 5 shows the addition of another set of vias 53 to the opposite polarity of plates, so that all plates are connected to plates of the same polarity.

[0024] FIG. 6 illustrates a detail of the vertical connectors 53. Plates 50-A belong to one of the first and second sets of plates. Plate 50-B belongs to the other set of plates. Plates 50 are formed by the same damascene technique, well known to those skilled in the art, that forms the other interconnects on this level. Vertical members 53-A are formed using the dual damascene technique simultaneously with plates 50-A. At the center of the Figure, plate 50-B is formed using the same damascene technique and simultaneously member 53-B is formed in aperture 51 and isolated from plate 50-B. Optionally, the top of member 53-B is widened, so that alignment tolerance is provided for the connection with upper member 53-A. The width of the widened member will be determined by the width of aperture 51 and the ground rules for the gap between 53-B and the walls of plate 50-B.

TABLE

Comparison of Capacitance Density					
FIG.	Structure Description	Area μm ²	Total Capaci- tance (fF)	Cap. Density (fF/μm ²)	Density Ratio to Structure 1
1	No Perforations	30	16.9779	0.566	N/A
2	18% perf., holes aligned	30	16.2798	0.543	0.959
3	18% perf., holes staggered	30	15.9160	0.531	0.938
4	18% perf., w/vert. vias, half plates staggered	30	19.3063	0.644	1.138
5	18% perf., w/vert. vias, all plates connected	30	22.4531	0.748	1.322
6	38% perf., holes aligned	30	15.0257	0.501	0.885

[0025] In all cases in Table I, the overlap area of the plates is 25 micron².

[0026] As can be seen in Table I, the perforated but unconnected version of FIG. 2 has 4.1% less capacitance density than the version of FIG. 1.

[0027] Similarly, the perforated and unconnected version of FIG. 3 also has less capacitance density than the embodi-

ment of FIG. 1. The aligned version of FIG. 1 benefits from the edge capacitance of the holes.

[0028] Connecting the vias improves the capacitance ratio substantially, as well as taking up less area after the removal of the vertical connection bars 56.

[0029] As can be seen from example 6 from table I, more perforation in copper plates results in lower capacitance. However, the loss in capacitance is much smaller than one skilled in the art would expect. When copper plates are perforated at 38%, the capacitance loss is approximately 11.5%.

[0030] The Figures show an even number of plates in the capacitor. Those skilled in the art will understand that an odd number of plates may also be used, so that the top and bottom plates will have the same polarity, e.g. ground.

[0031] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.

1. A parallel plate capacitor for use in an integrated circuit comprising a set of capacitor plates disposed on consecutive levels in the back end of an integrated circuit, alternate ones of the capacitor plates overlapping with vertically adjacent capacitor plates and being adapted to connect to electrical sources of opposite polarity, thereby forming a first set of a first polarity and a second set of a second polarity, said capacitor plates being formed simultaneously with other interconnections in the remaining portion of the integrated circuit; whereby said capacitor plates have the same thickness as said other interconnections and are separated vertically by the same amount of interlevel dielectric, in which:

each of said capacitor plates is a solid continuous layer, wherein at least one of said capacitor plates comprises a set of perforations formed within said solid continuous layer.

2. (canceled)

3. A capacitor according to claim 1, in which said perforations in said first set and in said second set are aligned vertically.

4. A capacitor according to claim 1, in which said perforations in said first set and in said second set are displaced horizontally, such that perforations in said first set are aligned vertically and perforations in said second set are aligned vertically at a different transverse location.

5. A capacitor according to claim 4, in which at least one pair of capacitor plates in one of said first and second sets are connected by vertical conductors passing through said aligned perforations of the other of said first and second sets, whereby said one pair of capacitor plates are connected.

6. A capacitor according to claim 5, in which all of the capacitor plates in one of said first and second sets are connected by vertical conductors.

7. A capacitor according to claim 5, in which at least one pair of capacitor plates in each of said first and second sets are connected by vertical conductors passing through said aligned perforations of the other of said first and second sets.

8. A capacitor according to claim 5, in which all pairs of capacitor plates in each of said first and second sets are connected by vertical conductors passing through said aligned perforations of the other of said first and second sets.

9. A method of forming a parallel plate capacitor comprising a set of capacitor plates disposed on consecutive levels in the back end of an integrated circuit, alternate ones of the capacitor plates overlapping with vertically adjacent capacitor plates and being adapted to connect to electrical sources of opposite polarity, thereby forming a first set of plates of a first polarity and a second set of plates of a second polarity, comprising the steps of:

depositing successively a set of capacitor levels of conductive interconnects in the back end of an integrated circuit, each of said capacitor levels including at least one conductive plate having the same thickness as other interconnect members on said capacitor levels and deposited simultaneously with said other interconnections.

10. A method according to claim 9, in which said capacitor plates are solid.

11. A method according to claim 9, in which said capacitor plates are perforated with a set of perforations having together a perforation area.

12. A method according to claim 9, in which each of said capacitor plates is perforated with a set of perforations having together a perforation area and at least one plate other than a top or bottom plate has vertical connection members passing through the apertures thereof and connecting to an upper plate above said at least one and to a lower plate below said at least one plate.

13. A method according to claim 11, in which said perforations in said first set and in said second set are aligned vertically.

14. A method according to claim 11, in which said perforations in said first set and in said second set are

displaced horizontally, whereby perforations in said first set are aligned vertically and perforations in said second set are aligned vertically at a different transverse location.

15. A method according to claim 12, in which at least one pair of capacitor plates of said first and second sets are connected by vertical conductors passing through said perforations of an intermediate plate of the other of said first and second sets, an upper part of said vertical connector being formed simultaneously with the upper plate of said pair of capacitor plates and a lower part of said vertical connector being formed simultaneously with said intermediate plate, whereby said pair of capacitor plates are connected.

16. A method according to claim 15, in which all of the capacitor plates in one of said first and second sets are connected by vertical conductors

17. A method according to claim 15, in which at least one pair of capacitor plates in each of said first and second sets are connected by vertical conductors passing through said aligned perforations of the other of said first and second sets.

18. A method according to claim 15, in which all pairs of capacitor plates in each of said first and second sets are connected by vertical conductors passing through said aligned perforations of the other of said first and second sets.

19. A method according to claim 15, in which all pairs of said first set are connected and all pairs of said second set are connected.

20. A capacitor according to claim 1, wherein said set of perforations is formed in a portion of said solid continuous layer which substantially overlaps at least one of a vertically adjacent capacitor plate.

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